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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/939,418	08/24/2001	Daniel J. Dove	10015055-1	4205

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EXAMINER	
KHUONG, LEE T	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 03/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/939,418	DOVE, DANIEL J.	
	Examiner	Art Unit	
	Lee Khuong	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because in line 7, the word "BMII" contains a typo error. It is suggested the word "BMII" to be changed to "GMII". Correction is required. See MPEP § 608.01(b).

2. The disclosure is objected to because of the following informalities: on page 2, line 11 and page 7, line 14, the words "13 pins" are suggested to be replaced with "12 pins".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-13 are rejected under 35 U.S.C. 102(e) as being anticipated by Chadha et al. (US 6,604,206) hereinafter is referred as Chadha.

Regarding claims 1, 8 and 13, Chadha teaches an apparatus, a media interface and a method for Reducing GMII With Internal Timing Compensation. Chadha teaches interfacing a

media access controller (MAC) (112, Fig. 2, ***MAC***) and a physical layer device (PHY) (108, Fig. 2, ***PHY***) in a manner whereby the standards of IEEE 802 are complied with for at least one of the gigabit media independent interface and the ten bit interface (see col. 2, line 46 – col. 3, line 2), transferring data at a predetermined rate while substantially reducing the required number of input and output pins (see col. 1, lines 45-58), said apparatus comprising: means for multiplexing the data and control signals that are normally applied to a predetermined number of pins to a significantly lesser number of pins and for selectively mapping the data and control signals to the lesser number of pins (see Fig. 2, col. 3, lines 13-49).

Regarding claim 2, Chadha teaches all limitations set forth in the rejection of claim 1. Chadha further teaches said multiplexing means multiplexes different significant bits of data on the same set of pins using both edges of a clock signal having the predetermined rate, thereby transferring data at the predetermined rate on the lesser number of pins (see col. 3, lines 13-49).

Regarding claim 3, Chadha teaches all limitations set forth in the rejection of claim 1. Chadha further teaches the clock rate is within the range of about 2.5 MHz and about 125 MHz, with the clock rate being within the range of about 2.5 and about 25 MHz for the ten bit interface and about 125 MHz for the gigabit media independent interface operation (see col. 3, lines 13-49).

Regarding claim 4, Chadha teaches all limitations set forth in the rejection of claim 1. Chadha further teaches said multiplexing means includes means for controlling the relative

timing between the clock signal and the data during transmitting and during receiving, the clock and data signals being generated substantially simultaneously when either the MAC or the PHY transmits the signals, such that the data to clock output skew at the transmitter is within +/-500 picoseconds and the data to clock input skew at the receiver is between about 1 and about 2.8 nanoseconds for clock signal speeds within the range of 2.5 MHz and 125 MHz (see Fig. 3, col. 3, lines 13-67).

Regarding claim 5, Chadha teaches all limitations set forth in the rejection of claim 3. Chadha further teaches the clock signal has a duty cycle for gigabit media independent interface operation that is within the range of 45 and 55 percent and a duty cycle for the ten bit interface operation that is within the range of 40 and 60 percent (see col. 5, line 29 – col. 6, line 4).

Regarding claims 6 and 10, Chadha teaches all limitations set forth in the rejection of claims 1 and 8. Chadha further teaches comprising six input pins (202, 204, 206, Fig. 2, ***six transmitting inputs***) for use in either the gigabit media independent interface operation or the ten bit interface operation in which: a transmit reference clock signal TXC is applied to a first pin in the gigabit media independent interface operation and the ten bit interface operation (202, Fig. 2, ***TXC***); 8 bits of data are applied to the second through fifth pins on both edges of a clock cycle during the gigabit media independent interface operation and the ten bit interface operation (see col. 3, lines 13-49, ***RGMII and RTBI shares four data path signals, the first four bits transmitted on the rising edge of the clock and the last four bits on the falling edge of the clock***); 2 bits of data are applied to the sixth pin in the ten bit interface operation (see

col. 3, lines 13-49); and, control signals are applied to the second through fifth pin in the gigabit media independent interface operation (see col. 3, lines 13-49).

Regarding claims 7 and 11, Chadha teaches all limitations set forth in the rejection of claims 1 and 8. Chadha further teaches six output pins (208, 210, 212, Fig. 2, ***six receiving outputs***) for use in either the gigabit media independent interface operation or the ten bit interface operation in which: a receive reference clock signal RXC is derived from the received data stream and appears on a first pin in the gigabit media independent interface operation and the ten bit interface operation (208, Fig. 2, ***RXC***); 8 bits of data are applied to the second through fifth pins on both edges of a clock cycle during the gigabit media independent interface operation and the ten bit interface operation (see col. 3, lines 13-49); 2 bits of data are applied to the sixth pin in the ten bit interface operation (see col. 3, lines 13-49); and, control signals are applied to the second through fifth pin in the gigabit media independent interface operation (see col. 3, lines 13-49).

Regarding claim 9, Chadha teaches all limitations set forth in the rejection of claim 8, wherein the reduced number of pins is 12 (see col. 3, line 21, ***reduced to 12 pins***).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chadha in view of Talaat et al. (US 6,115,364) hereinafter is referred as Talaat.

Regarding claim 12, Chadha teaches all limitations set forth in the rejection of claim 12.

Chadha does not expressly teach CRS and COL signals are applied on the same pin.

Talaat teaches CRS and COL signals are applied on the same pin (see Fig. 2, col. 2, line 59 – col. 3, line 28, ***share signals are transmitted on the same channel***).

At the time of the invention, it would have been obvious to one of ordinary skill in the art to employ the transmitting of CRS and COL signals on the same channel/pin of Tallat into the Reduced GMII of Chadha to arrive the invention of claim 12.

The suggestion/motivation for doing so would have been to provide a circuit and method for distributing shared signals that may reduce the number of pins required between a number of physical layer devices and a number of segments where the number of physical layer devices is greater than the number of segments (see col. 1, lines 39-45).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Muller et al. (US 6,044,087); Hey et al. (US 6,826,187); Sutardja et al. (US 6,816,505); Yu (US 2001/0043603) are cited to show a System and Method of Reduced Pin-Count Media Interface For Gigabit Ethernet Physical Layer Devices.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lee Khuong whose telephone number is 571-272-3157. The examiner can normally be reached on 9AM - 5PM.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lee T. Khuong
Examiner
Art Unit 2665

ALPUS H. HSU
PRIMARY EXAMINER